Claims 11-14

Applicant cannot find in Ormond "one or more planar perimeter side surfaces, each planar perimeter side surface extending between the first planar surface and the second planar surface", and "each planar perimeter side surface of the semiconductor die having a ground or polished surface" as recited in claim 11. Claims 12-14 depend from claim 11 such that they incorporate all of the limitations of claim 11. Therefore, Applicant respectfully requests allowance of claims 12-14 for the reasons provided above with regard to claim 11.

Applicant respectfully traverses the assertion at page 2 of the Office Action that each "semiconductor die taught by Ormond et al., like applicant, is shaped in a particular way such that die edges are not chipped or cracked or damaged [compare applicant's page 6, lines 6-19 with Ormond et al.'s, col. 4, lines 57-68]." Ormond appears to disclose using a dicing blade 60 to form edges 11 that intersect the sidewalls 35, 36 of grooves 33, 34. It appears that the side surfaces in Ormond are formed by edges 11 and grooves 40 (see FIGS. 4 and 5). It is unclear how Ormond teaches, among other things, ground or polished planar perimeter side surfaces that extend between the first planar surface and the second planar surface as recited in claim 11. By failing to teach such structure, Ormond does not meet the standard set forth in *In re Bond* requiring that "every element of the claimed invention must be identically shown in a single reference." 910 F.2d at 831, 15 USPQ2d at 1566, 1567.

The Office Action appears to be taking Official Notice of facts not supported by Ormond. Applicant traverses the Official Notice and respectfully requests a patent under MPEP § 2144.03 to support the assertion, or in the alternative, withdrawal of this assertion from the rejection.

The Office Action appears to admit that Ormond does not teach a ground surface. But, the Office Action maintained that this is inherent in Ormond because high speed dicing blade 60 inherently grinds away scribe material. Applicant respectfully disagrees because the Office Action has not

established a *prima facie* case of inherency because, as recited in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art," citing Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The Office Action only argued that in Ormond a high speed dicing blade 60 inherently grinds away scribe material.

Applicant respectfully submits that a polished or ground surface is not the same as a surface exposed by cutting. The specification in Ormond recognizes this at col. 1, lines 31-34, and col. 5, lines 15-22.

To serve as an anticipation when a reference is silent about the asserted inherent characteristic, the gap in the reference may be filled with recourse to extrinsic evidence. But, such evidence must make clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). Applicant respectfully submits that the Examiner has not produced extrinsic evidence to show that the a polished or ground surface is the same as a surface exposed by cutting.

Reconsideration and allowance of claims 11-14 is respectfully requested.

Claim 15-17

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond "one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending between the first planar surface and the second planar surface . . . the entire at least one perimeter side surface having a ground or polished surface" as recited in claim 15. Claims 16-17 depend from claim 15 such that they incorporate all of the limitations of claim 15. Therefore, Applicant

respectfully requests allowance of claims 16-17 for the reasons provided above with regard to claim 15.

FIG. 5 of Ormond appears to show that only a portion of the die's side surface is formed by groove 40. The dicing blade 60 cuts through tab 15 to form die 5 (see col. 6, lines 27-28) such that the entire side surface appears to formed by edge 11 and groove 40 with edge 11 including a surface exposed by cutting instead of a ground or polished surface as recited in claim 15.

Claim 18-21

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond where "at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other and ground or polished" as recited in claim 18. As stated above, edge 11 of Ormond appears to be a surface exposed by dicing blade 60.

Claims 19-21 depend from claim 18 such that they incorporate all of the limitations of claim 18. Therefore, Applicant respectfully requests allowance of claims 18-21 for the reasons provided above with regard to claim 18.

Claims 22-24

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond "one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending between the first planar surface and the second planar surface", and "means for treating the at least one planar perimeter side surface of the semiconductor die to provide the entire at least one planar perimeter side surface with a ground or polished surface" as recited in claim 22. Claims 23 and 24 depend from claim 22 such that they incorporate all of the limitations of claim 22. Therefore, Applicant respectfully requests allowance of claim 22-24 for the reasons provided above with regard to claim 22.

Applicant respectfully traverses the assertion that "regarding claim 22, the 'means' recited in the claim does not distinguish from any prior art semiconductor die since the mere 'existence of a die' is a 'means' to polish it [See MPEP 2113]. Page 4, Office Action. The Office Action appears to be taking Official Notice of facts not supported by Ormond. Applicant respectfully traverses this Official Notice and requests the Examiner to either 1.) cite references in support of this position pursuant to M.P.E.P. § 2144.03, or 2.) submit an affidavit as required by 37 C.F.R. § 1.104(d)(2) to support his position.

Reconsideration and allowance of claims 22-24 is respectfully requested.

Claim 25

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond where "each perimeter side surface having offset perimeter planar surfaces, where the perimeter planar surfaces are substantially parallel to each other, and each of the perimeter planar surfaces is a ground or polished surface" as recited in claim 25. Applicant respectfully notes that dicing blade 60 is used in every embodiment disclosed in Ormond. Ormond at col. 5, lines 15-19 recognizes that flaws exist in a surface exposed by cutting.

Reconsideration and allowance of claim 25 is respectfully requested.

Claims 35-40

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond where "at least one perimeter side surface having two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces, where the planar perimeter surfaces are substantially transverse to the first planar surface and the second planar surface" as recited in claim 35. Claims 36-40 depend from claim 35 such that they incorporate all of the limitations of claim 35. Therefore, Applicant respectfully requests allowance of claims 36-40 for the reasons provided above with regard to claim 35.

Claims 41-43

Applicant incorporates the above discussion of Ormond herein. Applicant cannot find in Ormond where "at least one perimeter edge having two or more offset planar surfaces, . . . each offset planar surface having a ground or polished surface" as recited in claim 41. As discussed above, it is unclear how Ormond teaches, among other things, that each offset planar surface is ground or polished when edge 11 in Ormond is exposed by cutting. By failing to teach such structure, Ormond does not meet the standard set forth in *In re Bond* requiring that "every element of the claimed invention must be identically shown in a single reference." 910 F.2d at 831, 15 USPQ2d at 1566, 1567.

Claims 42 and 43 depend from claim 41 such that they incorporate all of the limitations of claim 41. Therefore, Applicant respectfully requests allowance of claims 41-43 for the reasons provided above with regard to claims 41.

Applicant Comments on Advisory Action mailed July, 17, 2002

On page 3 of the Advisory Action the Examiner states that "cut edges of chips are desirably smooth, unchipped, and uncracked in the prior art (see col. 4, lines 57-60)." Applicant respectfully traverses the assertion. Applicant's specification (page 6, lines 6-26) and Ormond (col. 1, lines 31-34, and col. 5, lines 15-22) both recognize that cut edges are not the same as ground or polished edges. Applicant respectfully requests the Examiner to either 1.) cite references in support of this position pursuant to M.P.E.P. § 2144.03, or 2.) submit an affidavit as required by 37 C.F.R. § 1.104(d)(2) to support his position.

The Examiner further states at page 3 of the Advisory Action that "the examiner reasonably interprets the clean cut edges of the dice in Ormond et al. as being equivalent to 'polished' or 'smooth' edges since a high speed diamond blade cut followed by etch to relieve stresses is inherently a method of creating a super-smooth crystalline edge." Applicant respectfully traverses the accuracy of the examiner's assertion.

Applicant can not find any teaching or suggestion in Ormond as to cutting a die to expose a side surface and then etching the exposed side surface. As stated above, it appears in Ormond that the dicing blade 60 cuts through tab 15 to form die 5 (see col. 6, lines 27-28) such that the side surface is formed by edge 11 and groove 40 with edge 11 including a surface exposed by cutting instead of a ground or polished surface.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone **Applicant's attorney Andrew R. Peret at (262) 646-7009** to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date July 25, 2002 By _____
Catherine I. Klima-Silberg
Reg. No. 40,052

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 25th day of July, 2002.

Name Candis B. Buending

Signature _____

Clean Version of Pending Claims

GRINDLESS TECHNIQUE FOR INTEGRATED CIRCUITS
Applicant: Aaron M. Schoenfeld
Serial No.: 09/785,006

Sub G1 F1

11. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, each planar perimeter side surface extending between the first planar surface and the second planar surface;

a layer of scribe material forming the planar perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

each planar perimeter side surface of the semiconductor die having a ground or polished surface.

12. (Amended) The semiconductor die as recited in claim 11, wherein each planar perimeter side surface is transverse to the first planar surface and the second planar surface.

13. The semiconductor die as recited in claim 11, wherein the semiconductor die has a substantially rectangular shape.

14. (Amended) The semiconductor die as recited in claim 11, wherein each planar perimeter surface is a ground surface.

Sub G2

15. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending between the first planar surface and the second planar surface the entire at least one perimeter side surface having a ground or polished surface;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the first planar surface and the second planar surface of the semiconductor die have an overall rectangular shape.

16. (Amended) The semiconductor die as recited in claim 15, wherein each planar perimeter side surface is transverse to the first planar surface and the second planar surface.

17. (Amended) The semiconductor die as recited in claim 15, wherein each planar perimeter side surface comprises a polished surface.

18. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other and ground or polished.

19. The semiconductor die as recited in claim 18, wherein the semiconductor die comprises a rectangular die.

20. The semiconductor die as recited in claim 18, wherein each perimeter side surface has offset planar surfaces.

21. (Amended) The semiconductor die as recited in claim 18, wherein the at least two offset planar surfaces are transverse to the first planar surface and the second planar surface.

22. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending between the first planar surface and the second planar surface;

a layer of scribe material forming the planar perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

means for treating the at least one planar perimeter side surface of the semiconductor die to provide the at least one planar perimeter side surface with a ground or polished surface.

Sub C3

23.(Amended) The semiconductor die as recited in claim 22, wherein each of the entire planar perimeter side surfaces extends between the first planar surface and the second planar surface and is a ground or polished surface.

24. (Amended) The semiconductor die as recited in claim 22, wherein the at least one planar perimeter side surface is transverse to the first planar surface and the second planar surface.

25. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface;

each perimeter side surface having offset perimeter planar surfaces, where the perimeter planar surfaces are substantially parallel to each other, and each of the perimeter planar surfaces is a ground or polished surface ;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the semiconductor die has an overall rectangular footprint.

35. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter side surface having two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces, where the planar perimeter surfaces are substantially transverse to the first planar surface and the second planar surface.

36. (Amended) The semiconductor die as recited in claim 35, wherein each of the two or more offset planar perimeter surfaces is transverse to the first planar surface and the second planar surface .

37. The semiconductor die as recited in claim 35, wherein the semiconductor die has a substantially rectangular shape.

38. (Amended) The semiconductor die as recited in claim 35, wherein the two or more offset planar perimeter surfaces are parallel.

39. (Thrice Amended) The semiconductor die as recited in claim 35, wherein each of the two or more offset planar perimeter surfaces are polished surfaces.

40. (Amended) The semiconductor die as recited in claim 35, wherein each of the planar perimeter surfaces include two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces.

41. (Twice Amended) A semiconductor die comprising:

a first planar surface;

a second planar surface opposite the first planar surface;

one or more perimeter edges transverse to and extending between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface; and

each offset planar surface having a ground or polished surface.

42. The semiconductor die as recited in claim 41, wherein the semiconductor die comprises a rectangular die.

43. The semiconductor die as recited in claim 41, wherein the offset planar surfaces are substantially parallel to one another.